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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/982,595 | 10/18/2001 | Chong Chin Hui | TI-27874 | 7591 |

23494 7590 09/16/2003

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| EXAMINER |
|---|
| PAREKH, NITIN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application N . | Applicant(s) |
|---|---|---|
| | 09/982,595 | HUI ET AL. |
| | Examin r | Art Unit |
| | Nitin Parekh | 2811 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Peri d f r Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3,4,8,9 and 13-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,8,9 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Pri rity under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Claim Obj ctions*

1. Claim 14 is objected to because of the following informalities:

Claim 14, line 1: --- Insert "to the area of the die"--- between "regions" and "is".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura (US Pat. 5986333).

Regarding claim 8, Nakamura discloses a die pad (32 in Fig. 3-6) for an IC having an IC chip/die (22 in Fig. 6), the die pad comprising:

- a support portion substantially supporting all of the IC chip/die (see 32 in Fig. 3-6), and

- the support portion of the die pad being such that corner portions of the die pad have openings/slits (38 in Fig. 3-6) and the corner regions/portions of the chip/die are not in contact/supported by the die pad (see corners of the chip/die 22, slits 38 and die pad 32 in Fig. 3-6)

(Fig 3-6; Col. 4, line 20- Col. 5, line 65).

4. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Imamura et al. (US Pat. 5389817).

Regarding claim 13, Imamura et al. disclose a variety of die pad configurations (100, 110 and 120 in Fig. 8A-8C and 9A/B) for an IC chip/die (300 in Fig. 8A-8C and 9A/B), the die pad configurations comprising:

- the die/chip being rectangular and having two long and two short opposing edges (see the IC chip/die 300 in Fig. 8A-8C and 9A/B ), and
- two separate die pad regions (100a/110a/120a and 100b/110b/120b respectively in Fig. 8A-8C), each die pad region being under one of the two long opposing edges (see regions 100a/110a/120a and 100b/110b/120b being under the IC chip/die 300 in Fig. Fig. 8A-8C respectively)

(Fig 8A-8C and 9A/B; Col. 4, line 53- Col. 5, line 20).

***Claim Rejecti ns - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollingsworth et al. (US Pat. 5521428).

Regarding claim 1, Hollingsworth et al. disclose a die support structure having an integrated circuit (IC) die (65 in Fig. 6), the die support structure comprising a variety of die support configurations comprising:

- a plurality of die support/tie bar support regions including four separate die support regions/tie bar support regions (63 in Fig. 6), each die support /tie bar support region being under one of the corners of the IC die (see regions 63 overlapping 65 and 66 in Fig. 6), and
- the separated die support/tie bar support regions providing a reduced plastic/metal interface area to reduce delamination and stress/cracking related defects (Col. 6, line 5-65).

(Fig 6; Col. 6, line 25- 37; Col. 3-7).

Hollingsworth et al. fail to specify/designate the die support regions being the die pad regions.

Hollingsworth et al. further teach the support regions of the die support configuration providing a function of supporting the die or the dice having different sizes (Col. 3, lines 20-25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate four separate die support regions so that the delamination, void formation and stress/cracking related encapsulation defects can be reduced in Hollingsworth et al's die support structure.

Regarding claims 3 and 4, Hollingsworth et al. teach substantially the entire claimed structure as applied to claim 1 above, except ratio of the total area of the die pad regions to the die being in a range of about 0.3-0.5 or 0.32 respectively.

Hollingsworth et al. further teach selecting a variety of configurations for the die support regions having different shapes and sizes such as U-shape, H-shape, T-shape, segments having rounded edges, etc. to further reduce stress, improve support and to accommodate various die sizes/dimensions in the encapsulated package (Col. 6, line 25-47).

Furthermore, determination of parameters such as die support area, number of die support regions, thickness of the die pad/metal support, area ratio of die to die pad

support region, number of bonding wires/leads, encapsulant thickness, etc. and their effect the encapsulation defects such as delamination, void formation, cracking, etc. in chip packaging and encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired yield and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at the ratio of the total area of the die pad regions to the die being in the range of about 0.3-0.5 or 0.32 so that delamination, void formation and stress/cracking related defects can be reduced in Hollingsworth et al's die support structure.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (US Pat. 5986333) in view of Kelly et al. (US Pat. 5021864).

Regarding claim 9, Nakamura teach substantially the entire claimed structure as applied to claim 8 above, except a ration of the area of the support portion of the die pad to the area of the die being in a range of about 0.3-0.5.

Nakamura further teach selecting a variety of configurations/shapes for the slits/openings in the die pad including V-shape, U-shape, rectangular shape, etc. (see slits 48, 78, 79, etc. in Fig. 7, 12 and 13) to reduce the stress at the corners of the die pad and to reduce deformation of the leadframe package (Col. 3, line 30; Col. 5, line 15).

Kelly et al. teach a variety of die pad/paddle configurations (Fig. 5-14) having a range of area ratios of the die pad to the die including the die pad having openings at the corner regions (see die pad 3 in Fig. 13; Col. 3, lines 11-16) to provide the desired stress reduction for plastic packages (Col. 3, lines 11-16; Col. 1-3).

Furthermore, determination of parameters such as die support area, number of die support regions, thickness of the die pad/metal support, area ratio of die to die pad support region, number of bonding wires/leads, encapsulant thickness, etc. and their effect the encapsulation defects such as delamination, void formation, cracking, etc. in chip packaging and encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired yield and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at the ratio of the total area of the die pad regions to the die being in the range of about 0.3-0.5 as taught by Kelly et al. so that delamination, void formation and stress/cracking related defects can be reduced in Nakamura's die pad.

8. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imamura et al. (US Pat. 5389817).

Regarding claims 14 and 15, Imamura et al. teach substantially the entire claimed structure as applied to claim 13 above, except ratio of the total area of the die pad regions to the die being in a range of about 0.4-0.5 or 0.42 respectively.

Imamura et al. further teach in the embodiments of Fig. 8A-9B, the die pad regions having different areas, sizes and shapes (see regions 100a/110a/120a and 100b/110b/120b in Fig. Fig. 8A-8C respectively), the die pad configurations reducing thermal stress and voids/cracking defects in the package (Col. 4, line 50- Col. 5, line 7).

Furthermore, determination of parameters such as die support area, number of die support regions, thickness of the die pad/metal support, area ratio of die to die pad support region, number of bonding wires/leads, encapsulant thickness, etc. and their effect the encapsulation defects such as delamination, void formation, cracking, etc. in chip packaging and encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired yield and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to arrive at the ratio of the total area of the die pad regions to the die being in the range of about 0.4-0.5 or 0.42 so that delamination, void formation and stress/cracking related defects can be reduced in Imamura et al's die pad structure.

### *Response to Arguments*

9. Applicant's arguments filed on 06-16-03 have been fully considered but they are not persuasive.

A. Applicant contends that Hollingsworth et al. do not teach four die pad regions being under one of the four corners of the die.

However, as explained above, Hollingsworth et al. teach the support structure having four separate die support regions (63 in Fig. 6) functioning as the die support/die pad, each die support/tie bar support region being under one of the corners of the IC die (see regions 63 overlapping 65 and 66 in Fig. 6).

B. Applicant's arguments with respect to claims 8, 9 and 13-15 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
08-29-03

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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